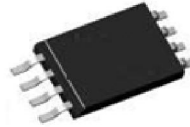
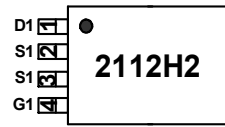


Main Product Characteristics

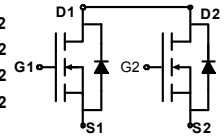
V_{DSS}	20V
$R_{DS(on)}$	10mohm(typ.)
I_D	8A



TSSOP-8



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced trench MOSFET process technology
- Special designed for battery protection, load switching and general power management
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature
- Lead free product



Description

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in battery protection, power switching application and a wide variety of other applications.

Absolute Max Rating

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I_D	8	A
	I_{DM}	50	A
Maximum Power Dissipation	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Resistance

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	°C/W
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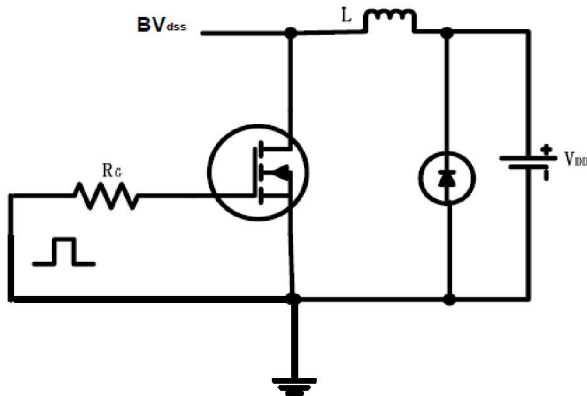


Electrical Characteristics @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

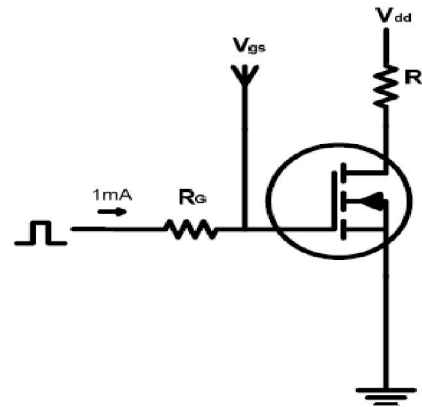
Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$			± 100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=4.5A$		10	12.5	m Ω
		$V_{GS}=2.5V, I_D=3.5A$		13.2	18.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=4A$	4			S
DYNAMIC CHARACTERISTICS (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=8V, V_{GS}=0V,$ $F=800KHz$		1520		PF
Output Capacitance	C_{oss}			229		PF
Reverse Transfer Capacitance	C_{rss}			198		PF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=1A$ $V_{GS}=4V, R_{GEN}=10\Omega$		18.3		nS
Turn-on Rise Time	t_r			4.8		nS
Turn-Off Delay Time	$t_{d(off)}$			43.5		nS
Turn-Off Fall Time	t_f			20		nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=4A,$ $V_{GS}=4V$		19		nC
Gate-Source Charge	Q_{gs}			4.2		nC
Gate-Drain Charge	Q_{gd}			4.9		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=2A$		0.67	1.2	V
Diode Forward Current (Note 2)	I_S				8	A

Test Circuits and Waveforms

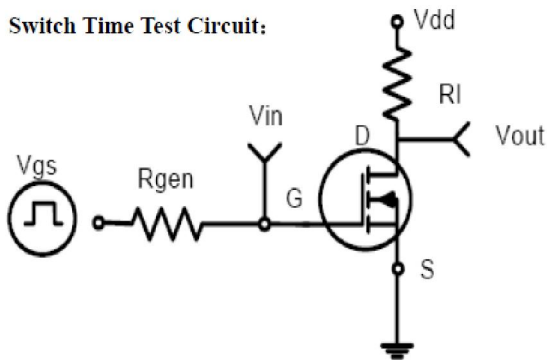
EAS test circuits:



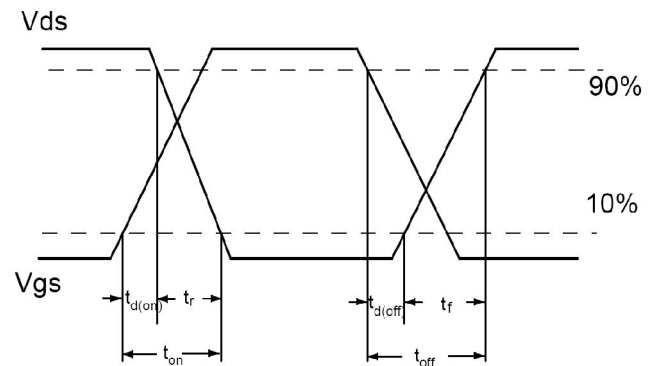
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production testing.

Typical Electrical and Thermal Characteristics

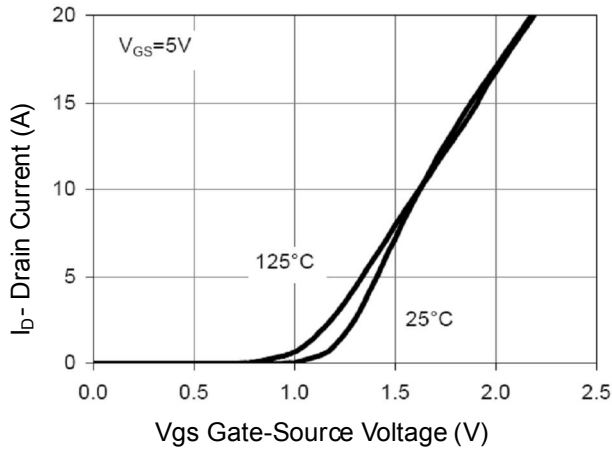


Figure 1: Transfer Characteristics

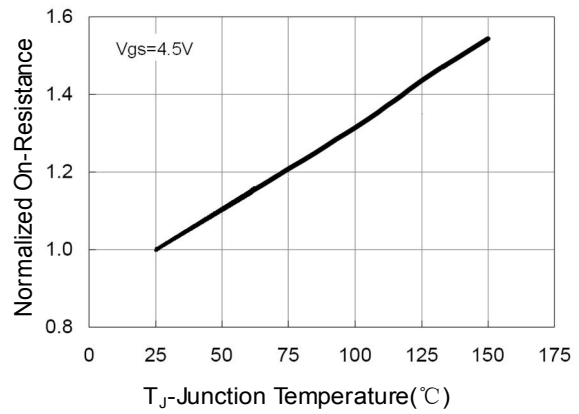


Figure 2: Drain-Source On-Resistance

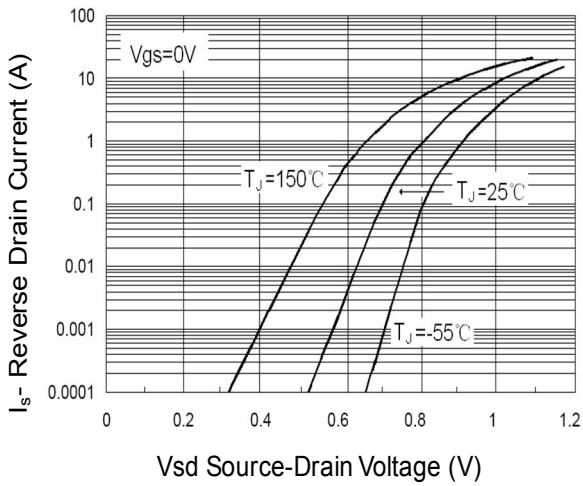


Figure 3 : Source- Drain Diode Forward

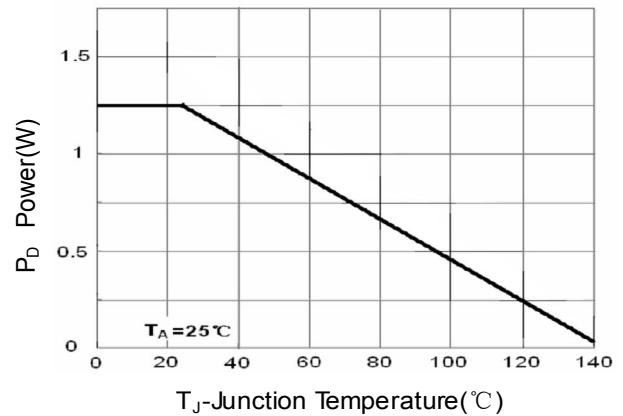


Figure 4: Power Dissipation

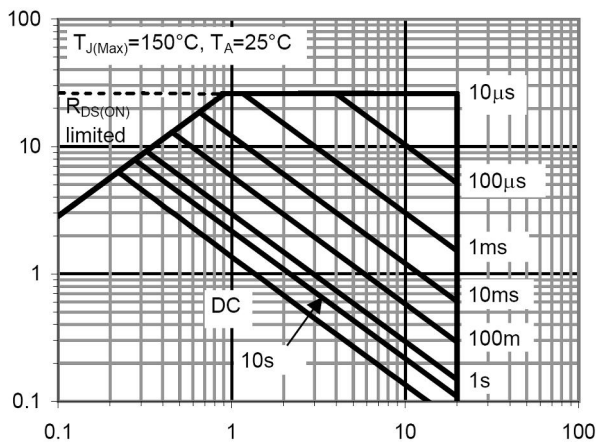


Figure 5: Safe Operation Area

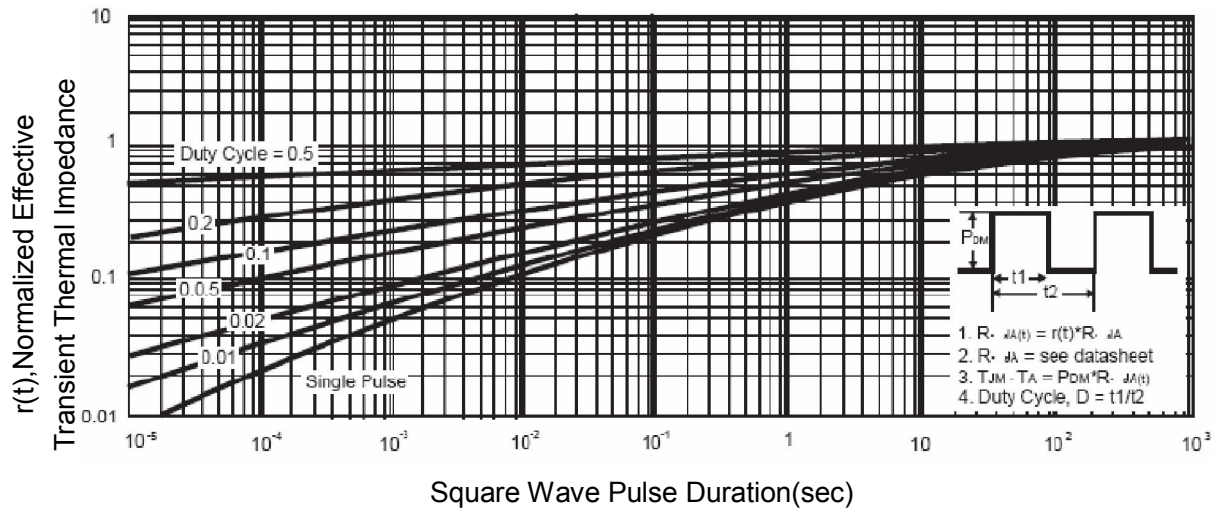
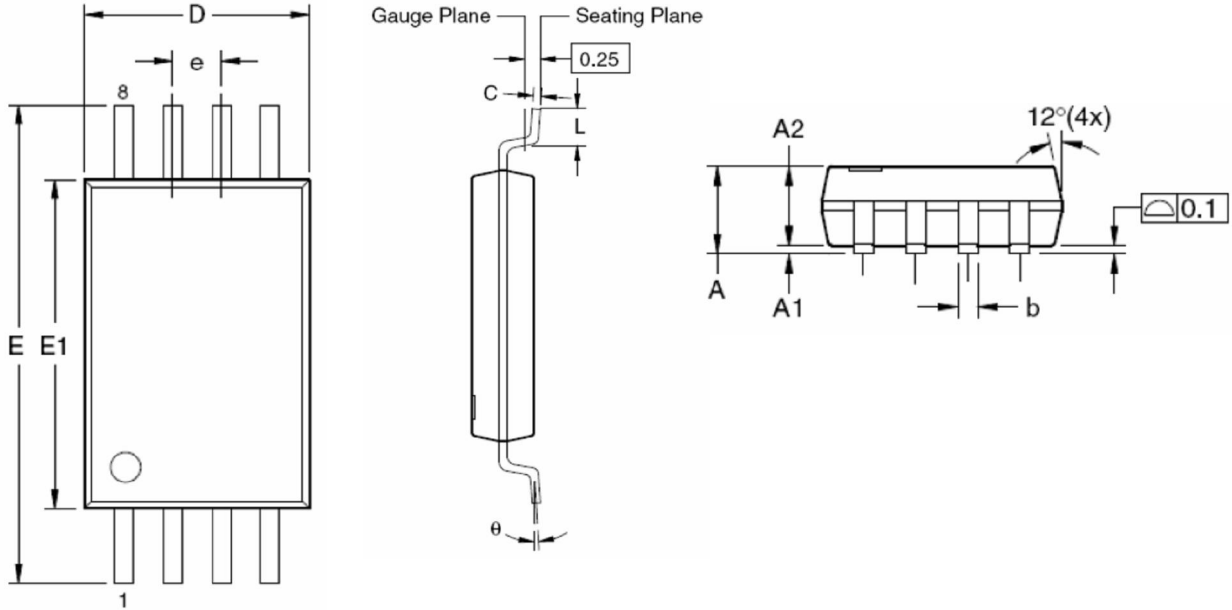


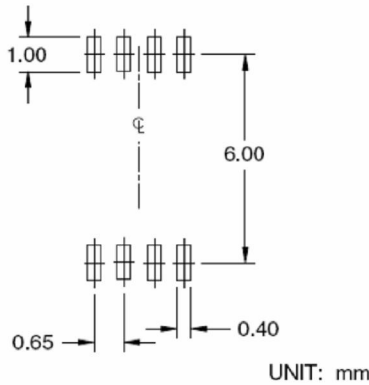
Figure 6: Normalized Maximum Transient Thermal Impedance

Mechanical Data

TSSOP-8 Dimensions in Millimeters (UNIT: mm)



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	2.90	3.00	3.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	—	—	0.047
A1	0.002	—	0.006
A2	0.031	0.039	0.041
b	0.007	—	0.012
C	0.004	—	0.008
D	0.114	0.118	0.122
E	0.252 BSC		
E1	0.169	0.173	0.177
e	0.026 BSC		
L	0.018	0.024	0.030
θ	0°	—	8°

NOTES:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.



SSF2112H2

20V Dual N-Channel MOSFET

Ordering and Marking Information

Device Marking: 2112H2

Package (Available)

TSSOP-8

Operating Temperature Range

C : -55 to 150 °C

Devices per Unit

Package Type	Units/ Tube	Tubes/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TSSOP-8	3000pcs	2pcs	6000pcs	8pcs	48000pcs

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ or 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ or 150°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices